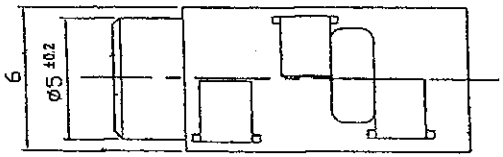
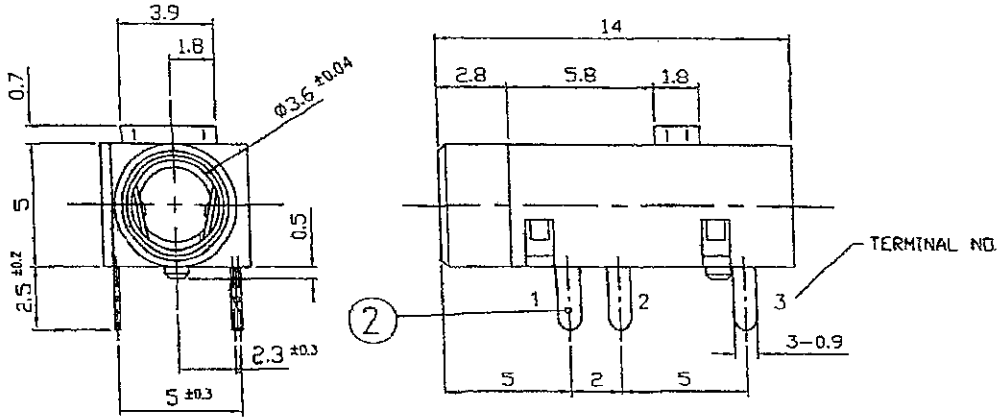
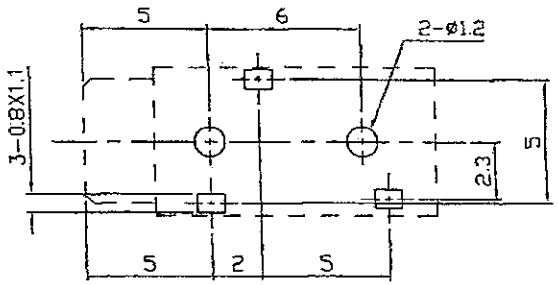


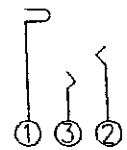
REVISION			
LTR	DESCRIPTION	DATE	APPROVED

控 制
CONTROLLED

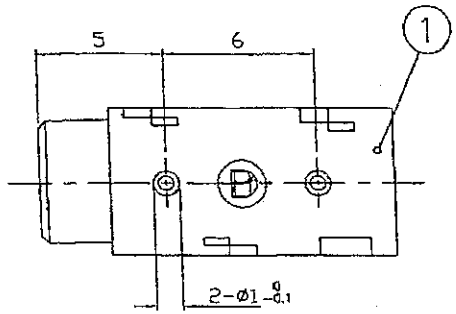




PC BOARD HOLE LAYOUT TOLS : ±0.1
(UPPER VIEW FROM DIRECTION OF INSERTION TO PCB)



CIRCUIT DIAGRAM



LET	PART NAME	QTY	MATERIAL	REMARK
2	TERMINAL	3	PBs 0.2t	Ag-PLATED
1	HOUSING	1	PC RESIN	SEE TABLE

TOLERANCES X <= 5 = ±0.10 X > 5 = ±0.30 ANGULAR = ±--- DO NOT SCALE DWG.	PART NAME STEREO EARPHONE JACK	
	MATL AS SHOWN IN TABLE	SCALE 4/1 mm
	DATE 09-10-2003	DRN / APPD CHEN / K.F.IM
FINISHED — — — —		

SHOGYO INTERNATIONAL CORP.

#MJ-0635